

TSMC-01-088B

January 28, 2004

To: Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/725,852 12/02/03

Yi-Hsun Wu et al.

AN EFFECTIVE Vcc TO Vss POWER ESD  
PROTECTION DEVICE

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.


The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents  
P.O. Box 1450, Alexandria, Va 22313-1450 on February 2, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 2/2/04

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U.S. Patent 5,898,205 to Lee, "Enhanced ESD Protection Circuitry," describes an ESD protection circuit using NMOS and PMOS devices.

U.S. Patent 5,953,601 to Shiue et al., "ESD Implantation Scheme for 0.35uM 3.3V 70A Gate Oxide Process," discloses an ESD implantation step using boron.

U.S. Patent 5,929,493 to Wu, "CMOS Transistors with Self-Aligned Planarization Twin-Well by Using Fewer Mask Counts," teaches a CMOS process using blanket, low dose boron implant to adjust  $V_{th}$  for ESD protection devices.

U.S. Patent 5,559,352 to Hsue et al., "ESD Protection Improvement," discloses a method to improve an ESD protection device using ion implantation.

Sincerely,

A handwritten signature in black ink, appearing to be 'SBA', written over a horizontal line.

Stephen B. Ackerman,  
Reg. No. 37761

